

A 0.18 μ m CMOS 2.45 GHz Low-Power Quadrature VCO with 15% Tuning Range

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Abstract — This work demonstrates the feasibility of a fully integrated LC-resonator based quadrature VCO for low power operation at 2.45 GHz, having a 15% tuning range due to a combination of analog and digital tuning techniques. The VCO dissipates 7.2 mW and fulfills the Bluetooth requirements. The design has been realized in a 0.18 μ m CMOS technology.

I. INTRODUCTION

Receiver architectures like zero-IF or low-IF offer flexibility and high integration. As in this type of I/Q-demodulation receivers' quadrature signals are needed, it is important to offer quadrature generation with minimal added power consumption.

Although several possibilities exist to generate quadrature signals, two techniques are commonly used. The first technique makes use of an oscillator at double the frequency followed by a divide-by-two circuit, which also generates the quadrature signal. This method is often applied in order to minimize pulling behavior between the power amplifier and the voltage-controlled oscillator (VCO). The second method relies on direct quadrature generation at the VCO output, where the VCO is operating at the required frequency. In recent years, the design of CMOS RF quadrature oscillators has gained interest [1-2].

This work demonstrates feasibility of a fully integrated LC-resonator based quadrature VCO for low power operation in the 2.45 GHz range, having a 15% tuning range due to a combination of analog and digital tuning techniques. The output signal swing is 1 V peak-to-peak, allowing to drive the mixers directly without need of any power consuming LO buffer. The VCO has been realized in a six metal 0.18 μ m CMOS technology on a 10 Ω cm substrate. The VCO fulfills the requirements for the Bluetooth communication standard.

Section II explains the tank design, while section III covers the design of the quadrature oscillator. Section IV explains the digital tuning mechanism. Measurement results are discussed in Section V, and we end up with some conclusions in section VI.

II. TANK DESIGN

The tank of the VCO has been built up around an inductor and a voltage-controlled capacitor. To achieve optimal performance, the total inductance is chosen to be 4.4 nH, setting thereby the maximum allowed capacitance to 900 fF. The differential inductor has been realized using two identical inductors, rather than designing a single symmetrical inductor. A better quality factor and higher resonance frequency were obtained at the expense of more silicon area.

The 3-turn planar spiral inductor uses the top three metal layers, while bridging is realized in metal 2 and 3. A grounded poly shield has been used to improve the performance. The shield is patterned with bars, where a ratio of 80 % has been used between bar width and bar distance. The physical structure was optimized using electro-magnetic field simulation. A microphotograph is shown in Figure 1. The measured unloaded quality factor of the inductor is 10 at 2.4 GHz (Figure 2).

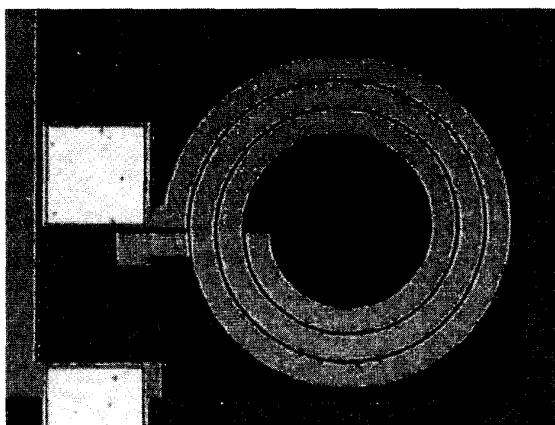


Figure 1. Die microphotograph of the used inductor in a test configuration.

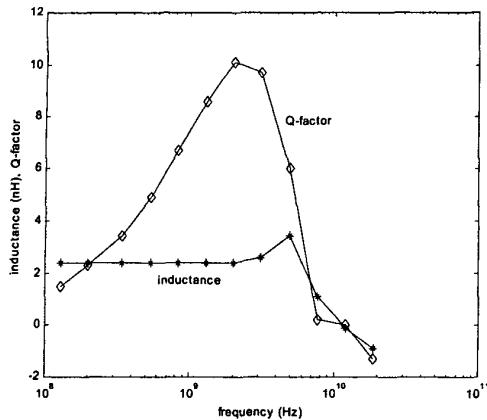


Figure 2. Measured inductance and quality factor of the inductor as function of the frequency.

The measured inductance is 2.2 nH and the resonance frequency is approximately 9 GHz. The extracted parasitic capacitance value of a single inductor is 123 fF, yielding 246 fF for two inductors and hence leaving approximately 650 fF for the tunable capacitor, parasitic capacitances and wire capacitance. Two identical NMOS devices were used to realize the tunable capacitor. The drain/source terminal capacitance of each NMOS negatively influences the noise performance if connected to the output nodes of the VCO, because the signal swing will change the total capacitance resulting in an asymmetry. Asymmetry increases the amount of noise that is up-converted from DC. Therefore the drain/source terminal is connected to the VCO control voltage. To reduce the gate resistance and improve the quality factor, the finger length of each MOS device has been set to 6 μ m. Width of the MOS device is 324 μ m and it has minimum length. The resulting maximum capacitance of the two MOS devices is 300 fF, leaving approximately 350 fF to be consumed by the active devices and wiring. The simulated C_{\max}/C_{\min} ratio is 1.7, which should lead to a tuning range of 200 MHz, enough to cover the Bluetooth band from 2.402 GHz to 2.480 GHz.

III. QUADRATURE GENERATION

A quadrature VCO can be obtained by cross-coupling two identical oscillator cores, resulting in a configuration as shown in Figure 3 [3]. VCO2 is connected to VCO1 in anti phase, while VCO1 is connected to VCO2 in common phase. This yields a 180-degree delay in phase from VCO2 output to VCO1 input, forcing the two VCO's to synchronize such that the phase delay in each is exactly 90

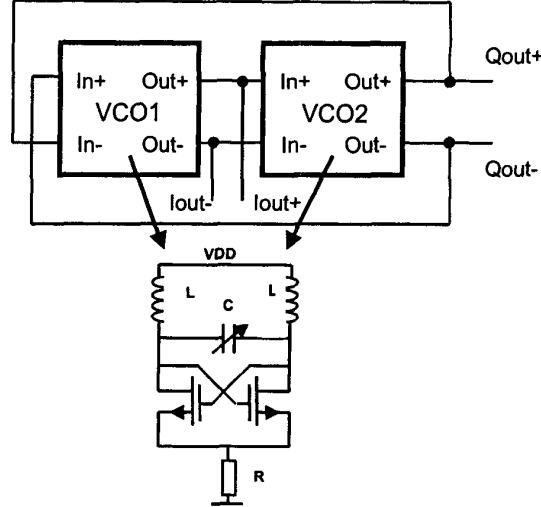


Figure 3. Block diagram of a quadrature VCO and schematic oscillator core.

degrees, assuming they are identical.

Each oscillator core has been designed as a fully differential basic negative- G_m LC oscillator (see Figure 3). The bias current of each oscillator is determined by a resistor R instead of using an NMOS device in combination with a current mirror configuration. The resistor contributes less noise than a current mirror with a high gain, needed to keep the power consumption low. A resistor also contributes less flicker noise. The chosen implementation means that no amplitude control is available. For the target application this is not a problem, as long as the output amplitude is more than 400 mV_{peak}. The value of the resistor is chosen such that the nominal DC level of the output signals is 1.25 V.

The MOS devices have minimum length and a width of 40 μ m. The device finger length has been optimized to minimize the gate resistance.

The quality factor Q_{tot} of the cross-coupled oscillator is approximately given by

$$Q_{\text{tot}} = 2Q_1 \cos(\alpha) \quad (1)$$

where α is the phase shift of the LC resonator in each stage with quality factor Q_1 [3,4]. The phase shift in each stage should therefore be zero for optimum phase noise. However, the implementation of Figure 3 results in a phase shift close to 80 degrees, resulting in a 12 dB degradation of the carrier-to-noise ratio. Inserting a zero in the transfer function of the coupling circuit enforces this condition. A common source amplifier with a capacitor C_c results in a

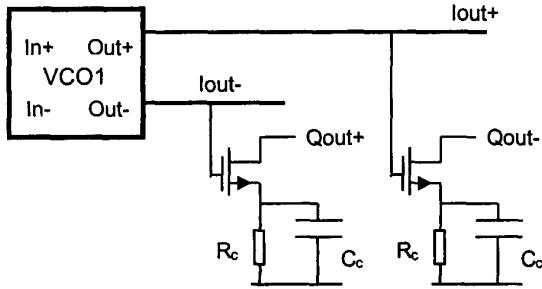


Figure 4. Coupling of I and Q path by means of an additional phase shift. A similar technique is needed for VCO2.

90-degree phase shift between the gate voltage and the drain current (Figure 4). The capacitor assures that the drain current of the MOS device has the same phase as the drain current in the oscillator core VCO2 and consequently optimum phase noise is reached. A similar coupling is used to connect VCO2 to VCO1. Because the currents have the same phase, the amplifier also drives the tank circuit in an optimal way. This method showed over 4dB improvement in phase noise during simulations. Finally, resistor R_c is needed for proper biasing of the amplifier.

IV. DIGITAL TUNING

The analogue tuning of 200 MHz or 8% can be enlarged by a digital tuning technique (Figure 5) without increasing the gain of the VCO. This additional tuning is needed to cope with process spread and production yield. The digital tuning will be used to set the VCO at the proper center frequency at initial start up. The analogue tuning will cover the channels and is controlled by the PLL. Both output nodes of the VCO cores VCO1 and VCO2 are loaded with 32 identical MOS devices implemented as a switched MOS capacitor bank. Each core will therefore

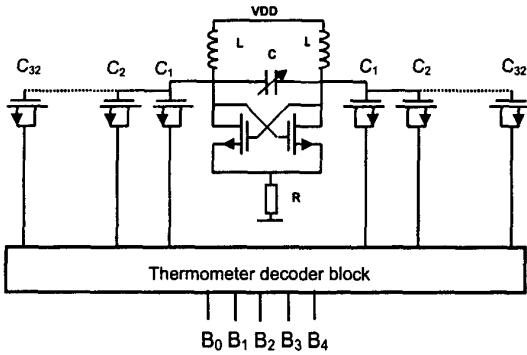


Figure 5. 32 MOS capacitors realize the digital tuning concept.

be loaded with 64 MOS capacitors. They are switched between 0 V and 1.8 V in a digital manner. A 5 bits thermometer decoder controls the ON/OFF state of these capacitors. The MOS capacitors are dimensioned with a W/L ratio of 9.8 μm /0.18 μm . These capacitors equate for an additional 200 MHz tuning range according to simulations.

V. MEASUREMENTS

A die microphotograph is shown in Figure 6. The die area is 742 μm x 742 μm and includes the VCO and the thermometer decoder. The die was mounted in a standard plastic, low cost, LQFP package. The complete quadrature VCO draws 4mA from a 1.8 V voltage supply. This 7.2 mW includes also the thermometer decoder block. The VCO core operates at 1.4 V supply. The oscillator operates from 2.370 GHz to 2.550 GHz, when the control voltage is swept from 0 V to 1.8 V for a '00000' digital setting. This means a 7% analog tuning range at a center frequency of 2.460 GHz. The '11111' setting gives a maximum frequency of 2.763 GHz, yielding 393 MHz or 15.3% overall tuning range at a center frequency of 2.567 GHz (Figure 7).

Measurements over 25 packaged samples indicate that the digital tuning range is large enough to cope with process spread, while the analogue tuning range can easily cover the Bluetooth band range when the VCO is properly tuned. Furthermore, measurements indicated that the analogue tuning range is not affected by the digital coded words.

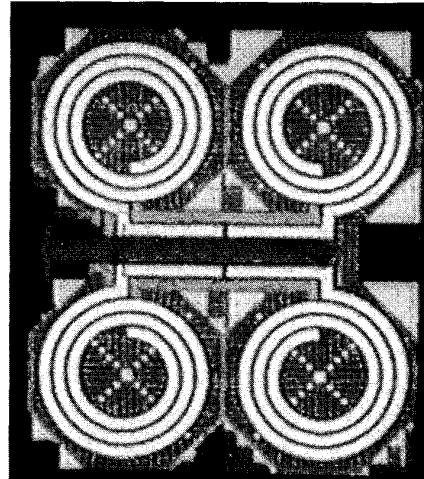


Figure 6. Die microphotograph of the VCO.

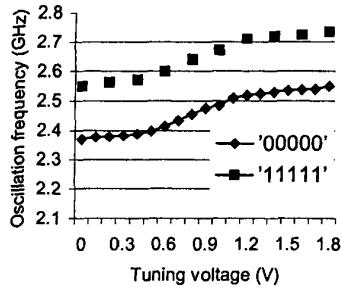


Figure 7. Measured tuning range of the VCO

Phase noise measurements were performed with an HP 3048 set-up and a Marconi 2042 low-noise signal generator as reference oscillator. The designed VCO has a phase noise of -115 dBc/Hz at 1 MHz, -120 dBc/Hz at 2 MHz and, -128 dBc/Hz at 3 MHz offset from 2.5 GHz, fulfilling therefore the Bluetooth requirements. Figure 8 shows the phase noise for the in-phase output, the quadrature output has a similar phase noise characteristic.

Finally the phase error has been measured with an Agilent FSIQ set-up. The measured error over several samples was less than 1.2 degrees. The amplitude error was less than 5 %, resulting in an image rejection ratio (IRR) of more than 50 dB, leaving enough design freedom for the mixers to achieve the overall Bluetooth specification of 20 dB IRR.

A well known FOM to compare VCO designs is defined as

$$FOM = S_{SSB} \cdot \left(\frac{f_{offset}}{f_c} \right)^2 P_{diss} (mW) \quad (2)$$

where S_{SSB} the single-sideband noise at offset frequency f_{offset} . Table 1 depicts the comparison results with the note that reference [6] is not a quadrature oscillator. We can conclude that the presented design has a comparable FOM value, but obtained at lower power consumption, higher frequency and extended tuning range. To the best of the authors knowledge this is the largest tuning range achieved, for a similar FOM-value.

VI. CONCLUSIONS

A fully integrated quadrature VCO with extended tuning range has been presented. The design dissipates 7.2 mW from a 1.8 V supply and has been realized in a standard 0.18 μ m CMOS technology. The performance achieved meets the Bluetooth requirements.

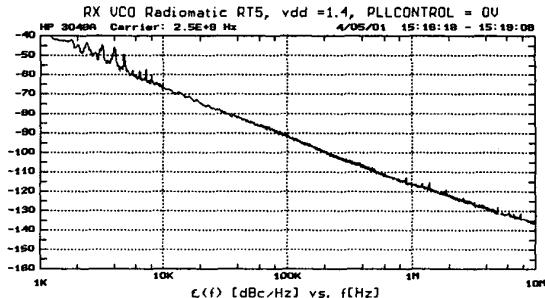


Figure 8. Measured phase noise of the in-phase output.

Table 1. Comparison of several CMOS quadrature VCO designs (except [6]).

Ref.	FOM (dBc)	Tuning range	f_c (GHz)	P_{diss} (mW)
[2]	-184	11 %	1.84	20
[4]	-179	9 %	1	13
[5]	-161	3.4 %	2.9	10
[6]	-185	10 %	2.45	3.8
This work	-178	15 %	2.45	7.2

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REFERENCES

- [1] B. Razavi, "A 1.8GHz CMOS Voltage-Controlled Oscillator", ISSCC Digest of Technical Papers, pp. 388-389, Feb., 1997
- [2] M. Tiebout, "A differential tuned 1.73GHz-1.99GHz Quadrature CMOS VCO for DECT, DCS1800 and GSM900 with a phase noise over tuning range between -128dBc/Hz and -137dBc/Hz at 600kHz offset", Proceedings ESSCIRC, pp.444-447, 2000
- [3] P. van de Ven, et. Al., "An optimally coupled 5 GHz quadrature LC oscillator," Symposium on VLSI, 2001, pp. 115-118
- [4] J.J. Kim, et. al., "A Low-Phase-Noise CMOS LC Oscillator with a ring structure," ISSCC Digest of Technical Papers, pp. 200-201, Feb., 2000
- [5] J.T. Hwang, et. al., "New High Performance and Wide Range Tunable Two-stage 3GHz CMOS RF Hetero-linked oscillators", proceedings ESSCIRC, pp. 354-357, 1999
- [6] D. Theil, et. al., "A fully Integrated CMOS Frequency Synthesizer for Bluetooth", proceedings RFIC, 2001